



Attorney Docket No. 42390.P8533

Patent

2D3
#6405
3-8-04
[Signature]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Jin Yang

Application No. 09/608,856

Filed: June 30, 2000

For: **METHODS FOR PERFORMING)
GENERALIZED TRAJECTORY)
EVALUATION**

) Examiner: ***

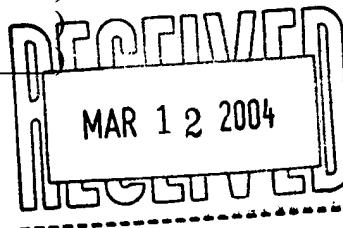
) Art Unit: 2123

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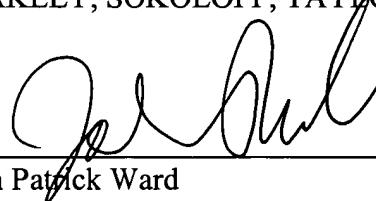
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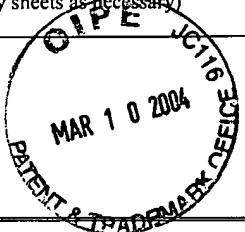
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: _____

3/5/04


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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42390.P8533	Application Number: 09/608,856
Sheet 1 of 1 		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123

OTHER ART – NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998	
		BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Volume 13, Issue 4, April 1994, pp. 401-424	
		CAMPOS, S.V.A., "Symbolic Model Checking in Practice," <u>XII Symposium on Integrated Circuits and Systems Design</u> , 1999 Natal, Brazil – IEEE, September 1999, pp. 98-101	
		HOJATI, R., et al., "Early Quantification and Partitioned Transition Relations," <u>1999 IEEE International Conference on Computer Design: VLSI in Computers and Processors</u> , 1996, ICCD '96 Proceedings - Austin, TX, October, 1996, pp. 12-19	
		ZHANG, ZHANG, "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <u>Proceedings of the Fourth Asian Test Symposium</u> , 1995 – Bangalore, India, November 1995, pp. 45-49	
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